WHAT IS CLAIMED IS:

Sub D1

1. A nonvolatile semiconductor memory device comprising:

a memory cell array having a plurality of memory cells arranged therein,

each said memory cell including a storage element holding binary data of n bits based on 2^n (n: natural number) threshold levels, and

said threshold levels respectively corresponding to ordered data obtained by rearranging a data set of said binary data of n bits in a procedure equivalent to steps of:

i) associating n bit pointer variables BP(i) (i: natural number, $1 \leqq i \leqq n$) with n integers from zero to (n – 1) arranged in arbitrary order respectively,

ii) dividing said data set into two data groups according to whether data of a BP(1)-th bit is "0" or "1" and arranging said two data groups in order in a first step, and

iii) dividng each of said data groups of said data set, which has been divided into 2^{j-1} groups in the process up to a (j – 1)th step, into two data groups further in response to whether data of a BP(j)-th bit is "0" or "1" in a j-th step (j: natural number, $2 \leqq j \leqq n$);

a cell selection circuit collectively selecting a plurality of said memory cells from said memory cell array in response to an address signal;

a data read/write circuit performing a read/write operation of storage data on said selected plurality of memory cells on the basis of $(2^n - 1)$ determination levels corresponding to boundaries between groups of said threshold levels corresponding to said data groups; and

a data input/output circuit for transferring said storage data between the outside of said nonvolatile semiconductor memory device and said memory cells as binary data through k input/output nodes by every k bit (k: natural number), wherein

storage data held in each said memory cell is generated from n bit data transferred at different timings through the same said input/output node.

2. The nonvolatile semiconductor memory device in accordance with claim 1, wherein

said n is two, and

$2^2 = 4$ said threshold levels correspond to elements "11", "10", "00" and "01" forming a set of 2-bit data respectively in ascending order.

3. The nonvolatile semiconductor memory device in accordance with claim 1, wherein

said data read/write circuit includes:

a first read data hold circuit for holding data read at said determination level for identifying said data of said BP(1)-th bit in said storage data held in said storage element and supplying said data to said data input/output circuit, and

a second read data hold circuit holding data read at said determination level for identifying said data of said BP(j)-th bit other than said BP(1)-th bit while said first data hold circuit performs data output to said input/output circuit.

4. The nonvolatile semiconductor memory device in accordance with claim 3, wherein

said data read/write circuit includes:

a read data identification circuit sequentially performing read operations at said determination levels for identifying bit data other than said BP(1)-th bit in said storage data from a period when said data input/output circuit outputs said data of said BP(1)-th bit in said storage data.

5. The nonvolatile semiconductor memory device in accordance with claim 4, wherein

said read data identification circuit includes:

a sense latch circuit holding said data read at said determination levels,

said first and second read data hold circuits are capable of

transferring said data held in said sense latch circuit, and

said nonvolatile semiconductor memory device further includes a read data conversion circuit converting data supplied to said data input/output circuit on the basis of data read at different said determination levels and held in said sense latch circuit and said first and second read data hold circuits.

6. The nonvolatile semiconductor memory device in accordance with claim 4, wherein

said read data identification circuit completes identification of said bit data other than said BP(1)-th bit in said storage data while said data input/output circuit outputs said data of said BP(1)-th bit in said storage data.

7. The nonvolatile semiconductor memory device in accordance with claim 5, wherein

said memory cell array includes:

a plurality of word lines connected to said memory cells belonging to a row of said memory cells,

said cell selection circuit selectively activates said word lines in response to said address signal, and

each of said first and second data hold circuits and said sense latch circuit is capable of collectively holding data of a memory cell selected every time each said word line is activated.

8. The nonvolatile semiconductor memory device in accordance with claim 1, wherein

the number of memory cells collectively selected by said cell selection circuit is m (m: natural number), and

said data read/write circuit performs data writing in said collectively selected m memory cells at said determination level for identifying said data of said BP(1)-th bit when first data of m bits are supplied among data of n by m bits sequentially supplied from said data input/output circuit to

be written in said collectively selected m memory cells.

9. The nonvolatile semiconductor memory device in accordance with claim 1, wherein

said data read/write circuit updates a value p (p: natural number) one by one from 1 every time data for m bits is supplied among data of n by m bits sequentially supplied from said data input/output circuit to be written in said collectively selected m memory cells and performs data writing in said collectively selected m memory cells at said determination level for identifying said data of said BP(p)-th bit.

10. The nonvolatile semiconductor memory device in accordance with claim 9, wherein

said data read/write circuit includes:

a plurality of write data hold circuits for holding said data for m bits respectively,

a sense latch circuit holding write conversion data in said collectively selected m memory cells at said determination level for identifying said data of said BP(p)-bit and performing writing, and

a write data conversion circuit for generating said write conversion data by an operation between said data held in said plurality of data hold circuits.

11. The nonvolatile semiconductor memory device in accordance with claim 10, wherein

said storage element is a floating gate transistor, and

said data read/write circuit selectively supplies a plurality of potential levels to drains of floating gate transistors of said collectively selected m memory cells for collectively performing writing at at least two of said determination level for identifying said data of said BP(p)-th bit.

12. The nonvolatile semiconductor memory device in accordance with claim 10, wherein

said sense latch circuit reads data written at said determination level for identifying data of said BP(p − 1)-th bit before performing writing at said determination level for identifying said data of said BP(p)-th bit, and

said write data conversion circuit generates said write conversion data by an operation between said data held in said sense latch circuit and said plurality of data hold circuits.

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